

FIG. 1A

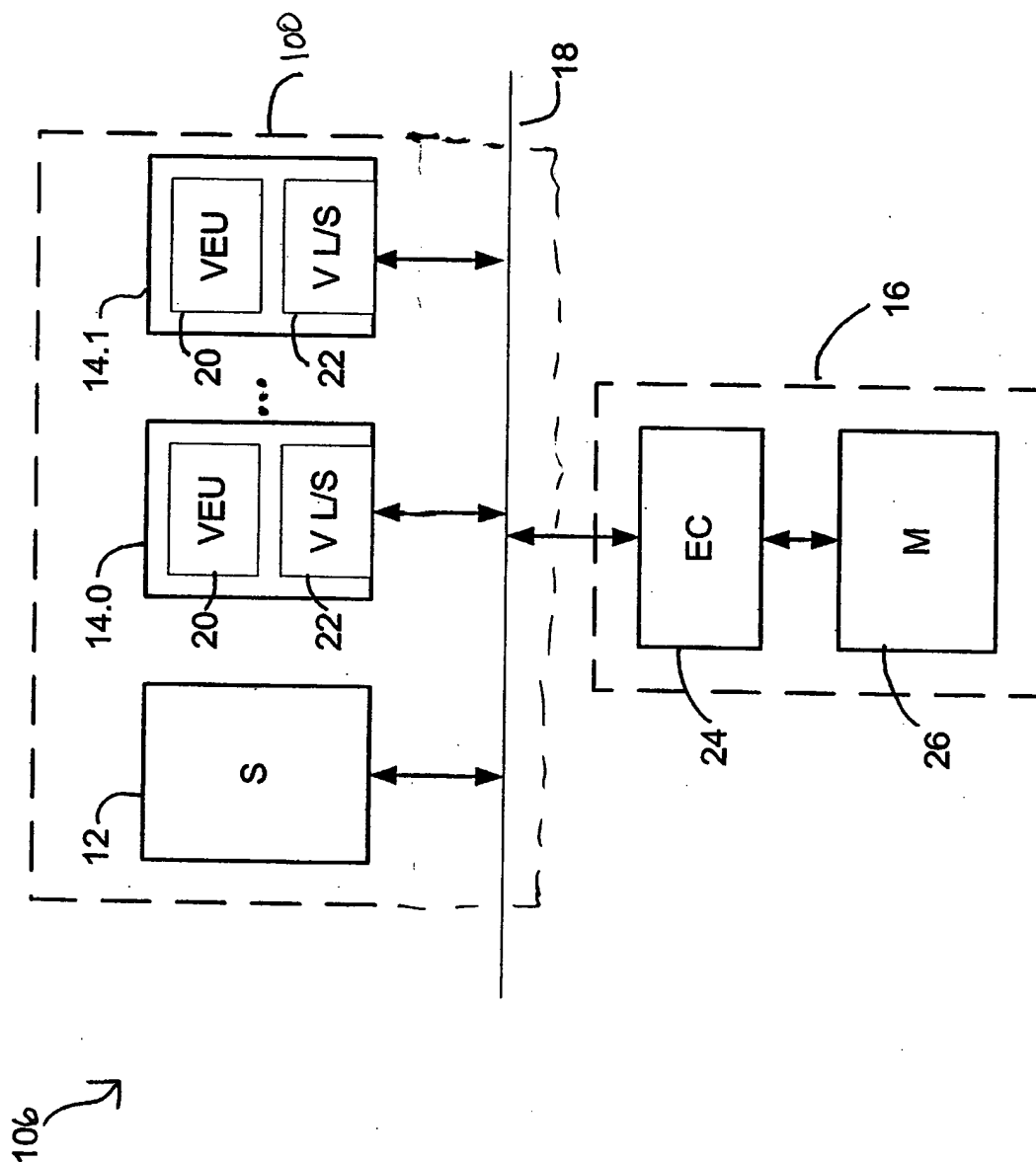
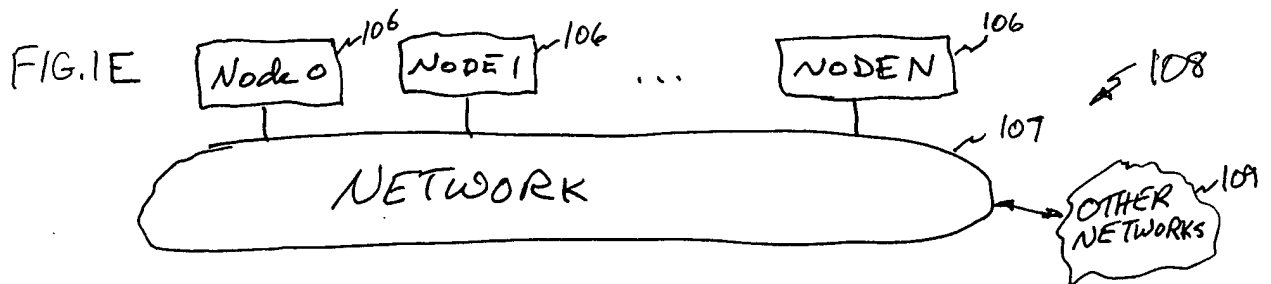
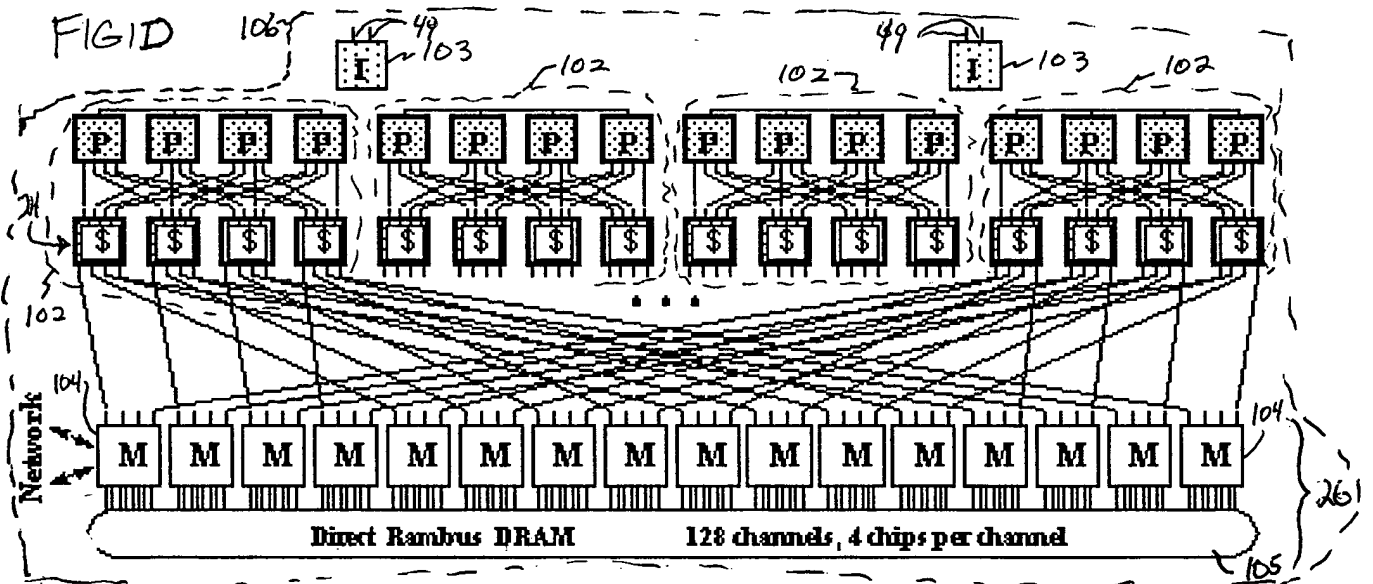
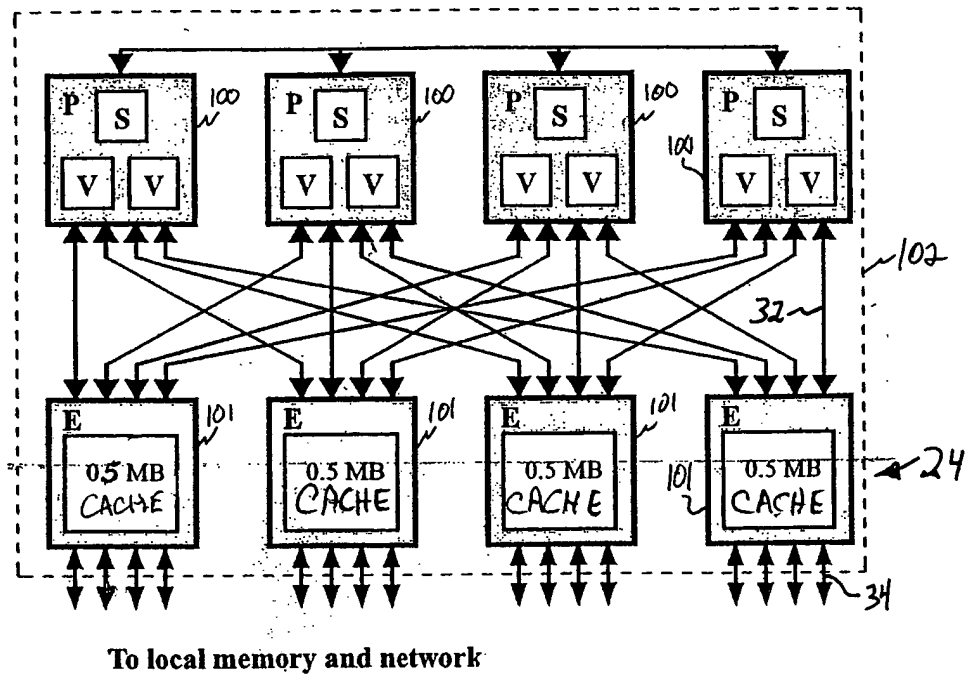


FIG. 1B

FIG. 1C



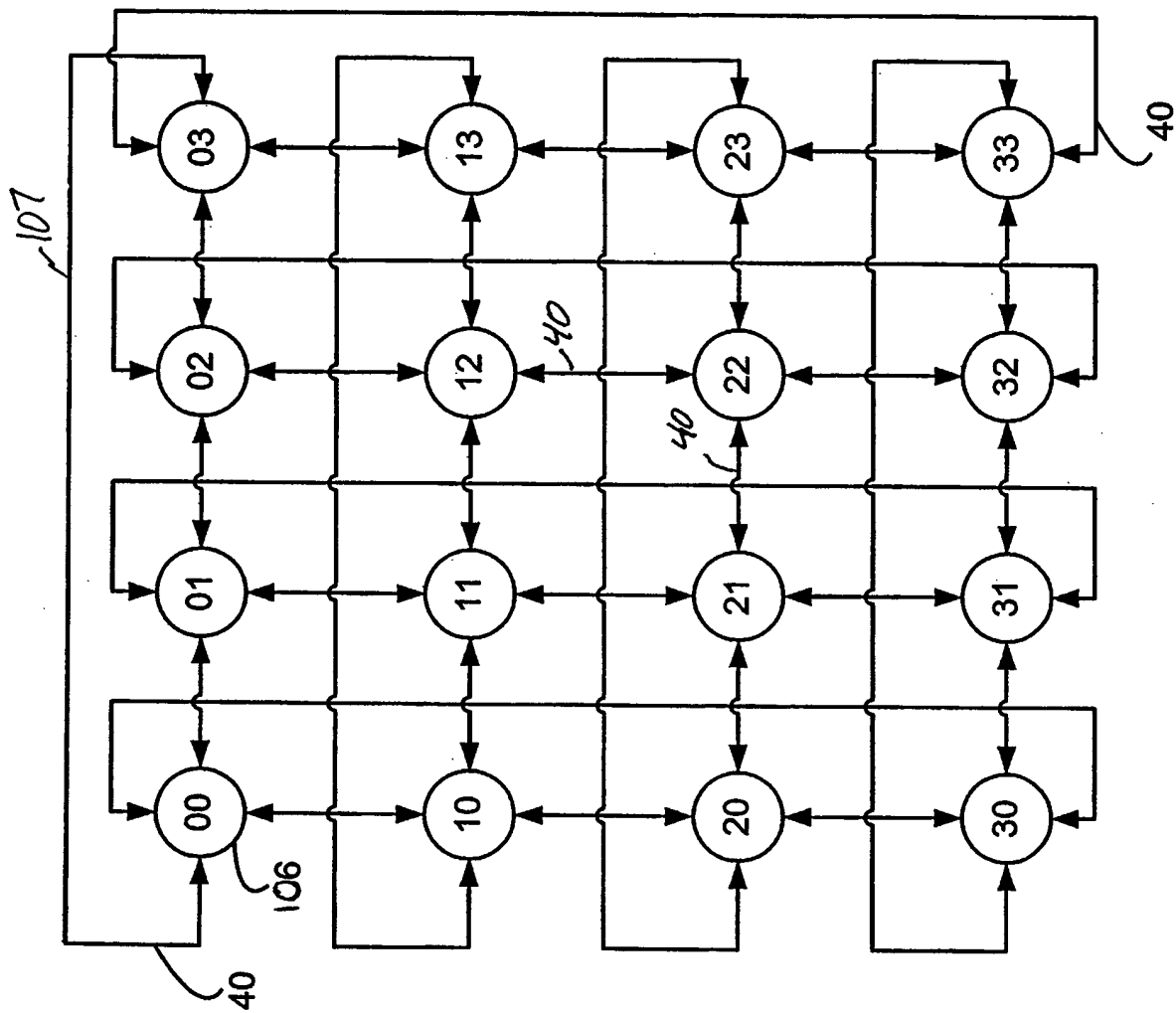


FIG. 1F

1002

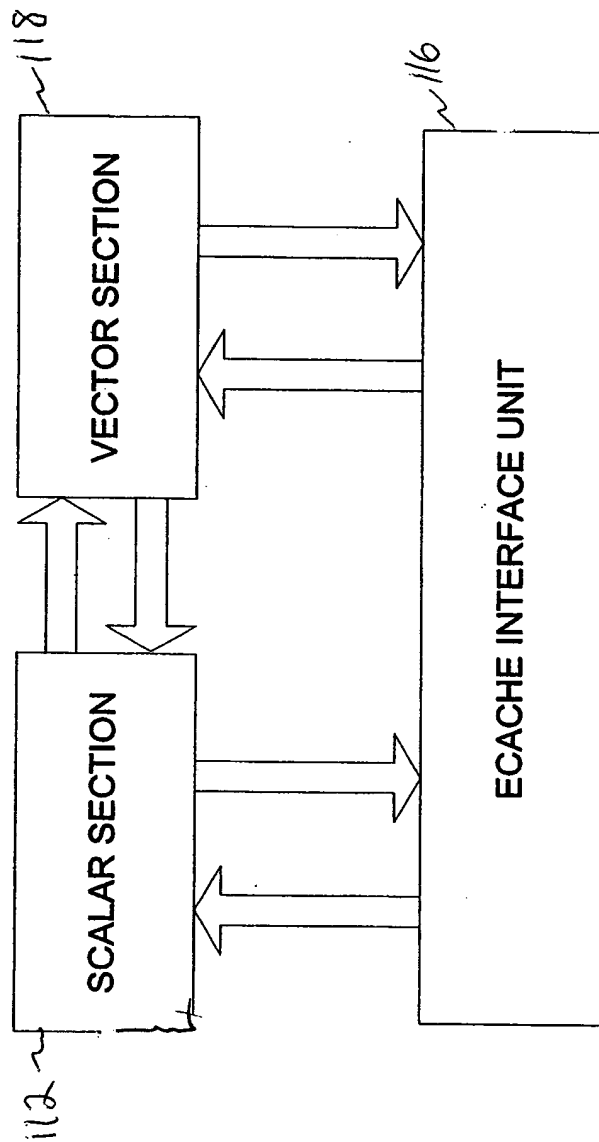


FIG. 1G

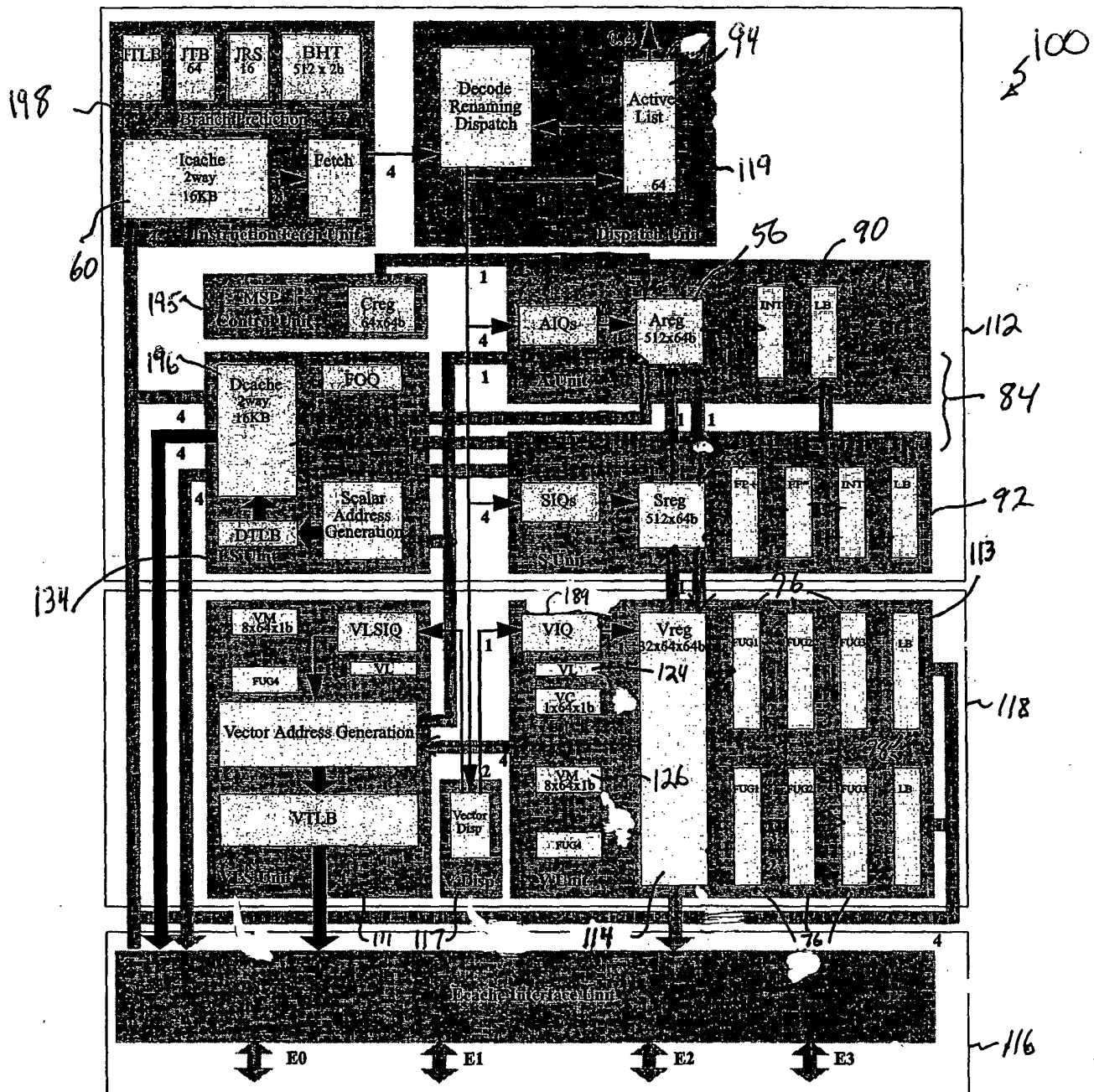


FIG. 1H

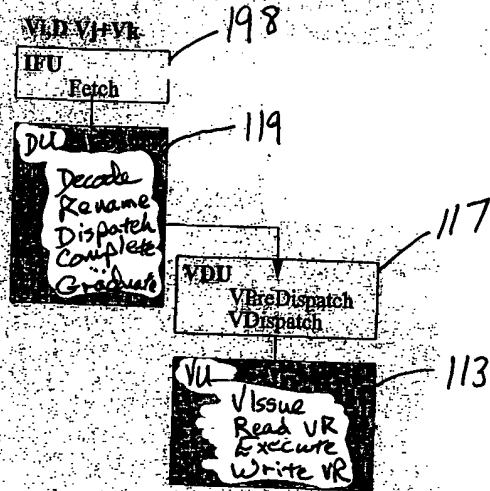


Fig. 11

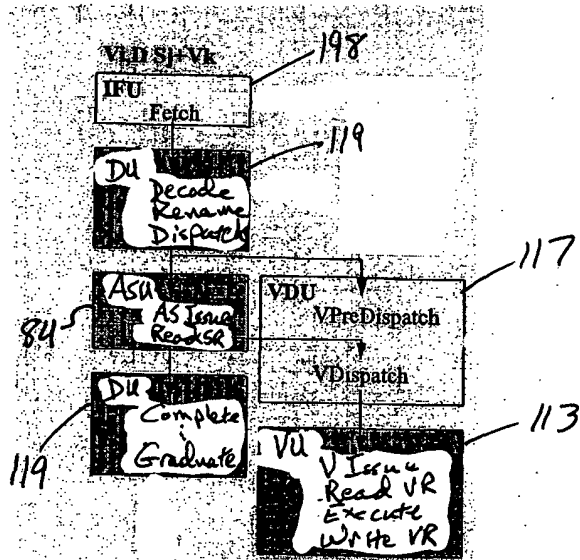
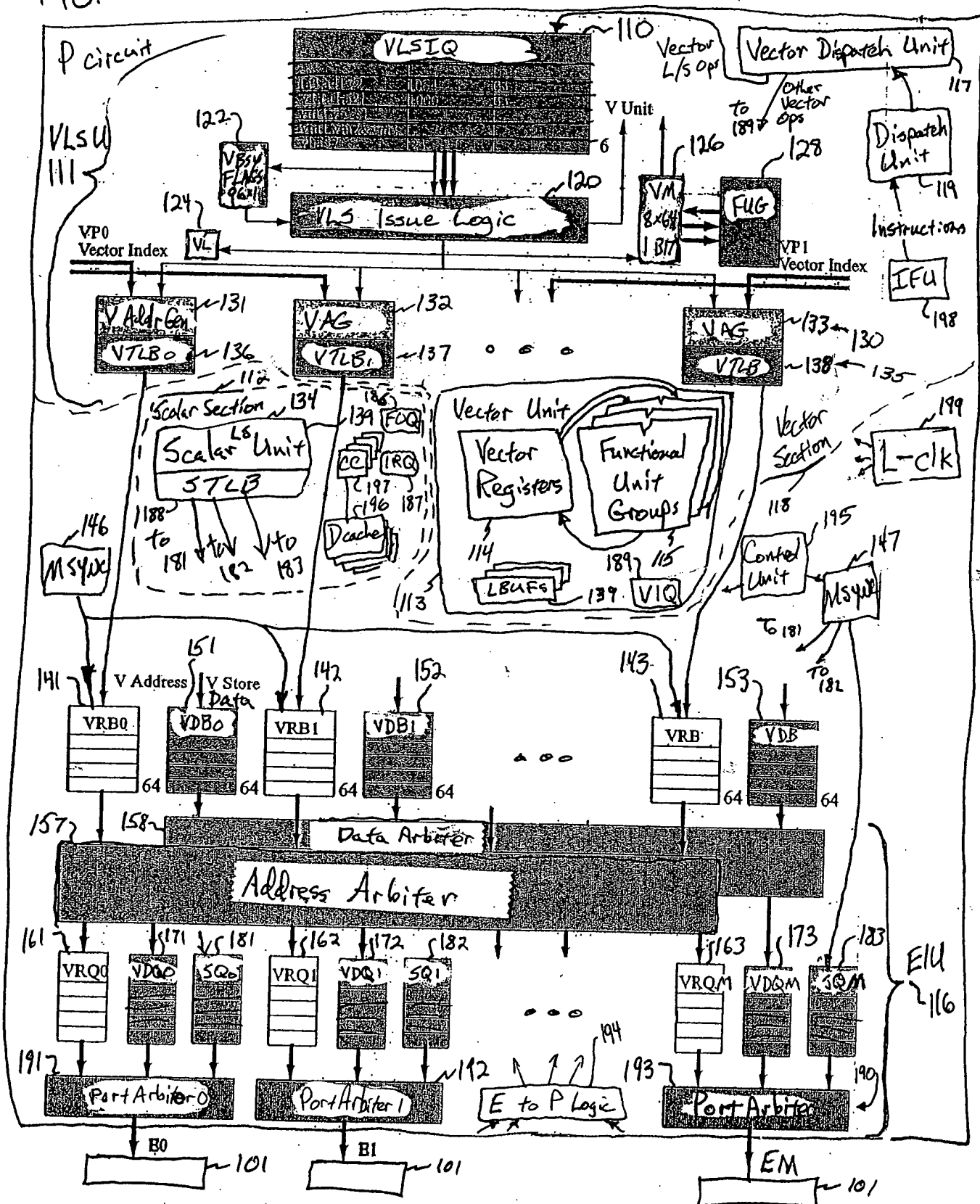


Fig. 1J

100



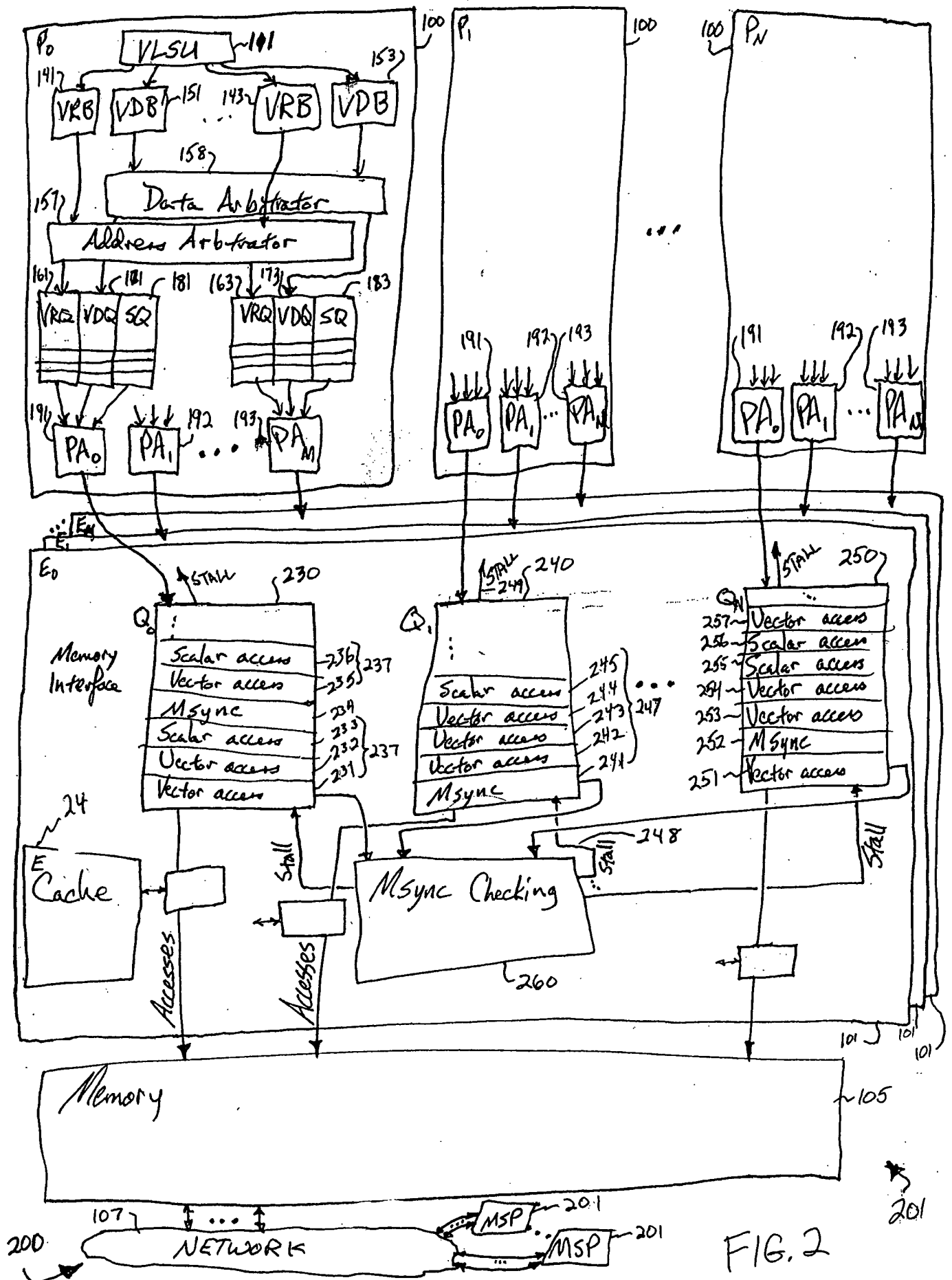


FIG. 2

FIG. 3

Vector Unit

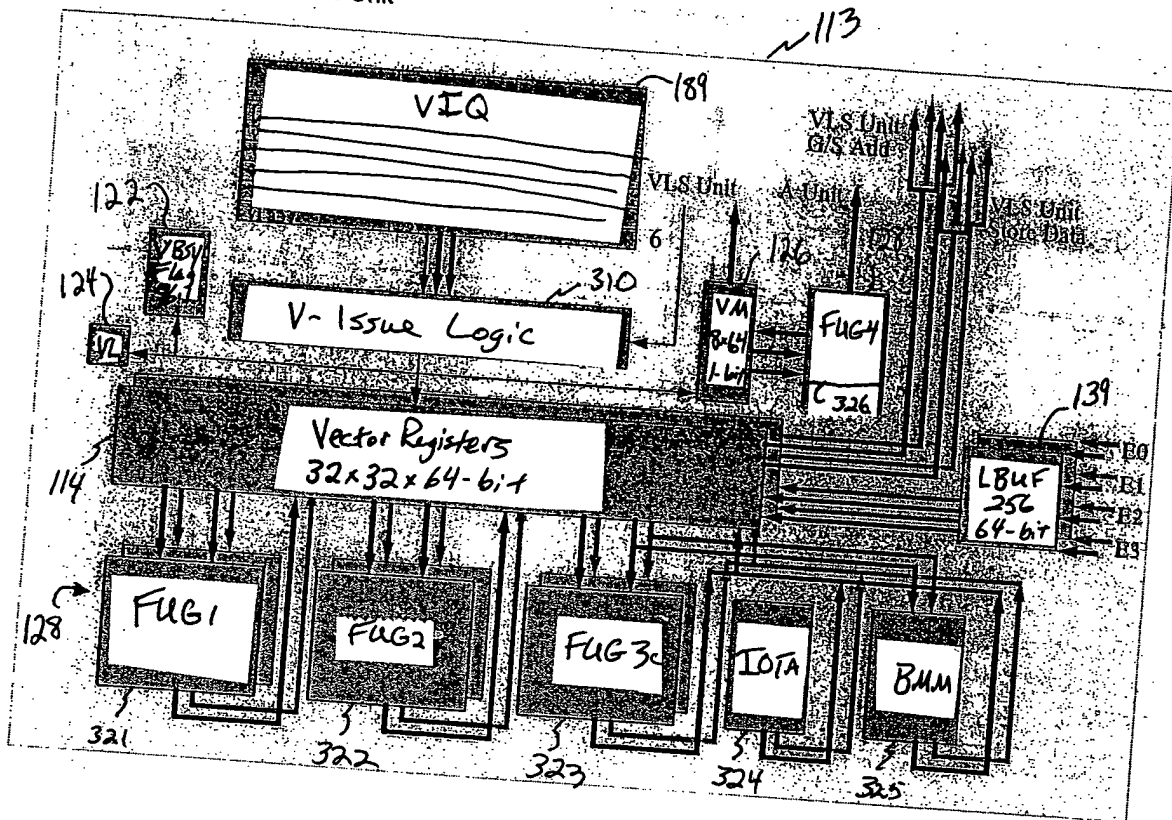
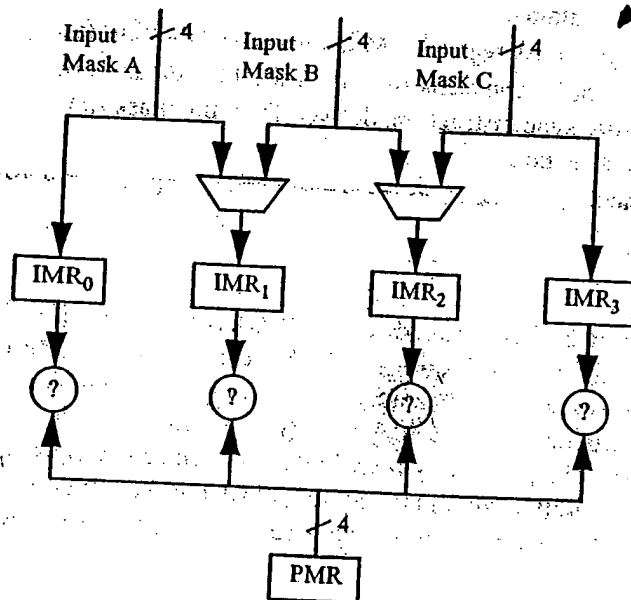


FIG. 4

M/Gsync logic block diagram



Muxing the inputs from the three other processors is controlled by the CPU field of the Config control register.

When there is an executing M/Gsync, a match is detected when all IMRs indicated by the PMR (except the IMR corresponding to the local P chip, which is ignored), match the bit pattern in the PMR. In this case, the Sync completes, and the PMR and participating IMRs are cleared.

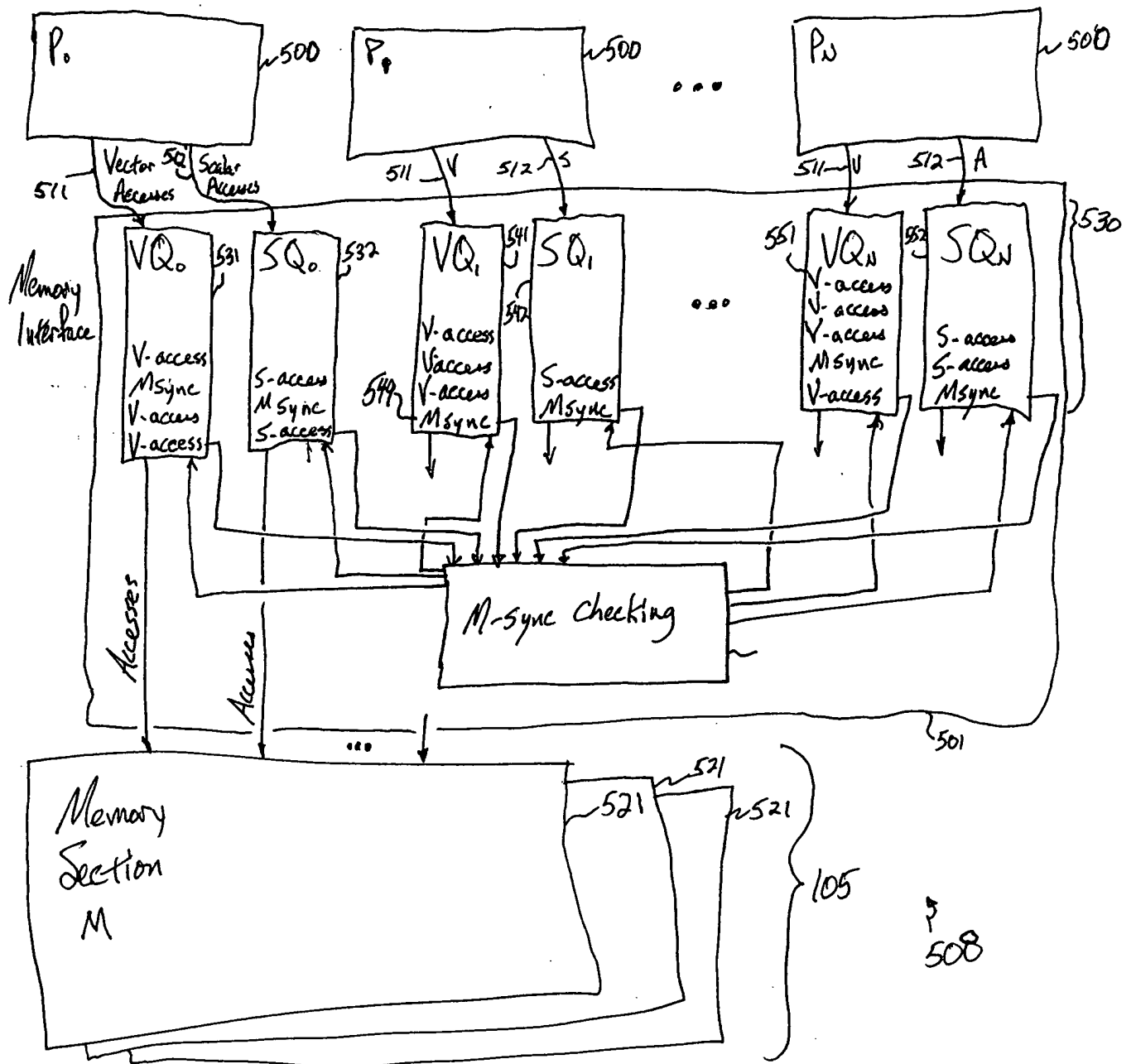


FIG. 5